REMARKS/ARGUMENTS

Applicant respectfully requests the consideration of the following remarks and the reconsideration of the present application.

The title was objected to for being not descriptive. The title is currently amended to be more descriptive.

Claims 1-66 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,446,198 (hereinafter "Sazegari"). Applicant respectfully disagrees.

Sazegari shows:

> "In accordance with the invention, multiple simultaneous lookups are carried out on a table that contains more than two registers of data, by performing permute operations on separate portions of the table, in combination with one or more select operations." (Col., 4, lines 59-60, Sazegari)

Thus, the multiple simultaneous lookups are carried out using "permute operations" ***and*** "one or more select operations". The description in the summary section of Sazegari (e.g., Col. 2, lines 17-43) is about such a method. Such a method is further illustrated in Figures 6 and 10. The description of the method of Figure 6 shows:

> "The same permute operation is carried out two times with respect to different sets of data represented by these four vectors. One permute operation selects data values from one set of data comprising vectors V_1 and V_2 in accordance with an index, or permute mask, and stores them in a result register V_{12}. The same permute mask is employed for another set of table data comprising vectors V_3 and V_4, and its results are stored in a second register V_{34}." (Col., 5, lines 2-10, Sazegari)

"The sixth bit of each byte in the index register is employed to identify whether the correct choice is in register V_{12} or register V_{34}." (Col., 5, lines 13-15, Sazegari)

"This is accomplished by first shifting the bits of each byte in the index to the left by two positions." (Col., 5, lines 16-17, Sazegari)

"After two shifts, the original value of the sixth bit occupies the most significant position in the byte. This bit value is then propagated throughout all of the other bit positions of the byte. One manner in which this can be done is to perform an arithmetic shift to the right seven times, as illustrated in FIGS. 8a-8h." (Col., 5, lines 21-26, Sazegari)

"This procedure is carried out for each byte in the index register, to thereby form a mask which can be used to select between the value stored in register V_{12} or register V_{34}." (Col., 5, lines 31-33, Sazegari)

Thus, the multiple simultaneous lookups of Figure 6 of Sazegari involve *two permute operations* to generate the results in registers V_{12} and V_{34} from the data in registers V_1, V_2, V_3, and V_4, *one shift* of the index register to the left by two positions followed by *one arithmetic shift* to the right seven times to generate the mask, and *one select operation* to finally generate the result in register V_R.

Figures 3 and 5 show the function representation of the permute instruction and the select instruction respectively (see, e.g., Col. 2, lines 61-67, Sazegari).

Further, the abstract of Sazegari shows:

"A lookup operation is carried out on a data table by logically dividing the data table into a number of smaller sets of data that can be indexed with a single byte of data. Each set of data consists of two vectors, which constitute

the operands for a permute instruction. ... The remaining bits of each index are used as masks into a series of select instructions. ..." (abstract, Sazegari)

Thus, from the description of Sazegari, one understands that a computer code including a set of vectorized instructions can be used to perform the lookup operations in a vectorized fashion. The computer code would include instructions, such as one permute instruction for each data set stored in two vector registers as illustrated in Figure 3, a series of select instructions each of which is illustrated in Figure 5, a shift instruction and an arithmetic shift for each selection instruction, etc.

However, for example, claim 1 recites:

1. (Original) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
receiving a string of bits;
generating a plurality of indices using a plurality of segments of bits in the string of bits;
looking up simultaneously a plurality of entries from a plurality of look-up tables using the plurality of indices; and
combining the plurality of entries into a first result;
wherein the above operations are performed in response to the microprocessor receiving the single instruction.

The operations recited in claim 1 are performed "in response to the microprocessor receiving the ***single*** instruction". The method of Sazegari as described in the summary section of Sazegari (e.g., Col. 2, lines 17-43) involves a code of multiple instructions. Thus, what is claimed in claim 1 is clearly different from the method of Sazegari.

The permutation instruction of Figure 3 of Sazegari may be considered as a look up operation. However, the permutation instruction is clearly different from what is claimed in claim 1. Figure 4 of Sazegari illustrates the look up operations of the permute instruction. From Figure 4, it is seen clearly that multiple indices (36) are used in ***one same*** look up table (34) to look up the results in register 38. However, claim 1 recites the limitation of "looking up simultaneously a plurality of entries from ***a plurality of look-up tables*** using the plurality of indices".

Thus, at least for the above reasons, Sazegari does not anticipate claim 1.

Independent claim 34 recites similar limitations as claim 1; dependent claims of claims 1 and 34 incorporate the limitations of the corresponding independent claims through dependency. Thus, as least for the above reasons, Sazegari does not anticipate claims 1-66.

Applicant respectfully submits that the pending claims are patentable over the cited references.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

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Date: 3/14, 2005

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